

Abstract of the disclosure

A digital control variable delay circuit includes n amplitude control units which are connected in parallel and each of which receives a pair of input clock signals to be supplied to a differential pair and receives m -bit digital control signals, and a waveform shaping unit which is connected to the outputs of the n amplitude control units. Each amplitude control unit is capable of varying the amplitude of each of the pair of clock signals into $(m + 1)$ values using the m -bit digital control signals, and outputs a pair of amplitude-varied clock signals. The waveform shaping unit receives a pair of added clock signals obtained by adding and combining the pairs of amplitude-varied clock signals outputted from the n amplitude control units and outputs a pair of resultant clock signals as output signals.